STATUS OF THE CLAIMS

This listing shows the current state of the claims in the application.

Listing of Claims:

1. (previously presented) A processor comprising:

a first pipeline having a first number of stages to process instructions;

a second pipeline having a second number of stages, which is greater than the first number of stages, to process floating point instructions; and

a control circuit coupled to the first and second pipelines to inhibit co-issuance of a first instruction to the first pipeline, if a second instruction to be issued to the second pipeline is a floating point instruction and the first instruction is subsequent to the second instruction in program order, the first instruction to be inhibited for a predetermined number of stage cycles until the first instruction is determined not to graduate from the first pipeline at least no earlier than the second instruction reaching a stage in the second pipeline where exceptions are to be generated to ensure that the first instruction does not graduate from the first pipeline prior to exception determination for the second instruction in the second pipeline.

2. (previously presented) The processor as recited in claim 1 wherein the control circuit can disable generation of exceptions.

3. (previously presented) The processor as recited in claim 1 wherein the second instruction is a long latency floating point instruction.

4. (previously presented) The processor as recited in claim 1 wherein the first instruction is an integer instruction and the first pipeline is an integer pipeline.

5. (previously presented) The processor as recited in claim 1 wherein the first instruction is a load/store instruction and the first pipeline is a load/store pipeline.

6. (previously presented) The processor as recited in claim 1 wherein the second instruction is a floating point multiply-add instruction.

7-8. (canceled)

9. (previously presented) The processor as recited in claim 1 further comprising a scoreboard coupled to the control circuit and the scoreboard includes a set of scoreboard registers to maintain scoreboarding of pending reads and writes.

10. (previously presented) The processor as recited in claim 9 wherein the scoreboard uses bits for the scoreboard registers to indicate that a write is pending.

11. (previously presented) A method comprising:

queuing a first instruction for issuance to a first pipeline having a first number of stages;

queuing a second instruction, which is a floating point instruction, for issuance to a second pipeline having a second number of stages, which is greater than the first number of stages, to process floating point instructions;

issuing the second instruction to the second pipeline; and

inhibiting co-issuance of the first instruction to the first pipeline, if the first instruction is subsequent to the second instruction in program order, the first instruction to be inhibited for a predetermined number of stage cycles until the first instruction is determined not to graduate from the first pipeline at least no earlier than the second instruction reaching a stage in the second pipeline where exceptions are to be generated to ensure that the first instruction does not graduate from the first pipeline prior to exception determination for the second instruction in the second pipeline.

12. (previously presented) The method as recited in claim 11 further including selective disabling of exceptions in the second pipeline.

13. (previously presented) The method as recited in claim 11 wherein queuing the

second instruction queues a long latency floating point instruction.

14. (previously presented) The method as recited in claim 11 wherein queuing the first instruction queues an integer instruction and the first pipeline is an integer pipeline.

15. (previously presented) The method as recited in claim 11 wherein queuing the first instruction queues a load/store instruction and the first pipeline is a load/store pipeline.

16. (previously presented) The method as recited in claim 11 wherein queuing the second instruction queues a multiply-add instruction.

17-18. (canceled)

19. (previously presented) The method as recited in claim 11 further comprising scoreboarding to maintain pending reads and writes pending in the pipelines.

20. (previously presented) A carrier medium comprising one or more data structures representing a processor, the processor including:

a first pipeline having a first number of stages to process instructions;

a second pipeline having a second number of stages, which is greater than the first number of stages, to process floating point instructions; and

a control circuit coupled to the first and second pipelines to inhibit co-issuance of a first instruction to the first pipeline, if a second instruction to be issued to the second pipeline is a floating point instruction and the first instruction is subsequent to the second instruction in program order, the first instruction to be inhibited for a predetermined number of stage cycles until the first instruction is determined not to graduate from the first pipeline at least no earlier than the second instruction reaching a stage in the second pipeline where exceptions are to be generated to ensure that the first instruction does not graduate from the first pipeline prior to exception determination for the second instruction in the second pipeline.